AMENDMENTS TO THE CLAIMS:

This listing of the claims will replace all prior versions, and listings, of the claims in this application.

Listing of Claims:

1. (Original) A multi-mode Input/Output (I/O) circuit for transmitting and receiving data between integrated circuits (ICs), wherein each IC contains at least one of said I/O circuits, comprising at least one of transmitter circuitry or receiver circuitry, said transmitter circuitry sending data to receiver circuitry in another IC, and said receiver circuitry receiving data from transmitter circuitry in another IC, said I/O circuit being constructed with CMOS-based transistors that are selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, or as a single differential current or voltage mode link.

2. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry sends data to said receiver circuitry in another IC over a first pair of adjacently disposed conductors, and where said receiver circuitry receives data from said transmitter circuitry in another IC over a second pair of adjacently disposed conductors.

3. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating under a condition where a power supply voltage of said transmitter circuitry is equal to a power supply voltage of said receiver circuitry in another IC, for operating under a condition where the power supply voltage of said transmitter circuitry is less than the power supply voltage of said receiver circuitry in another IC, and for operating under a condition where the power supply voltage of said transmitter circuitry is greater than the power supply voltage of said receiver circuitry in another IC.

4. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in one of a plurality of

double single-ended, CMOS voltage level link modes, wherein in a first mode a power supply voltage of said transmitter circuitry is equal to a power supply voltage of said receiver circuitry in another IC, wherein in a second mode the power supply voltage of said transmitter circuitry is less than the power supply voltage of said receiver circuitry in another IC, and wherein in a third mode the power supply voltage of said transmitter circuitry is greater than the power supply voltage of said receiver circuitry in another IC.

5. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in one of said plurality of double single-ended, CMOS voltage level link modes, or in said differential voltage or current mode links, and wherein the ICs at each end of the link may operate with different supply voltages.

6. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a double single-ended voltage mode link mode.

7. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a double single-ended current mode link mode.

8. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a mode defined by a single differential voltage mode link with a single-ended input drive.

9. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a mode defined by a single differential voltage mode link with a differential input drive.

10. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said

receiver circuitry are selectively configured by switches for operating in a mode defined by a single differential current mode link with a single-ended input drive mode.

11. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a mode defined by single differential current mode link with a differential input drive.

12. (Original) A multi-mode I/O circuit as in claim 1, wherein certain switches are provided to convert said I/O circuitry into either said transmitter circuitry configuration or into said receiver circuitry configuration.

13. (Original) A method for transmitting and receiving data between integrated circuits (ICs) that comprise a portable radiocommunication device, comprising:

providing at least two ICs to each contain at least one I/O circuit, said I/O circuit comprising at least one of transmitter circuitry or receiver circuitry, the transmitter circuitry sending data to receiver circuitry in another IC, and the receiver circuitry receiving data from transmitter circuitry in another IC, the I/O circuit being constructed with CMOS-based transistors; and

selectively interconnecting together the CMOS-based transistors with switches to operate as two single-ended, current or voltage mode links, or as a single differential current or voltage mode link.

14. (Original) A method as in claim 13, wherein said transmitter circuitry sends data to said receiver circuitry in another IC over a first pair of adjacently disposed conductors, and where said receiver circuitry receives data from said transmitter circuitry in another IC over a second pair of adjacently disposed conductors.

15. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver

circuitry are selectively configured by the switches for operating under a condition where a power supply voltage of said transmitter circuitry is equal to a power supply voltage of said receiver circuitry in another IC, for operating under a condition where the power supply voltage of said transmitter circuitry is less than the power supply voltage of said receiver circuitry in another IC, and for operating under a condition where the power supply voltage of said transmitter circuitry is greater than the power supply voltage of said receiver circuitry in another IC

16. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in one of a plurality of double single-ended, CMOS voltage level link modes, wherein in a first mode a power supply voltage of said transmitter circuitry is equal to a power supply voltage of said receiver circuitry in another IC, wherein in a second mode the power supply voltage of said transmitter circuitry is less than the power supply voltage of said receiver circuitry in another IC, and wherein in a third mode the power supply voltage of said transmitter circuitry is greater than the power supply voltage of said receiver circuitry in another IC.

17. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by the switches for operating in a double single-ended voltage mode link mode.

18. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by the switches for operating in a double single-ended current mode link mode.

19. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by the switches for operating in a mode defined by a single differential voltage mode link with a single-ended input drive.

20. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by the switches for operating in a mode defined by a single

differential voltage mode link with a differential input drive.

21. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by the switches for operating in a mode defined by a single differential current mode link with a single-ended input drive mode.

22. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by the switches for operating in a mode defined by single differential current mode link with a differential input drive.

23. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by said switches for operating in one of said plurality of double single-ended, CMOS voltage level link modes, or in said differential voltage or current mode links, and wherein the ICs at each end of the link may operate with different supply voltages.

24. (Original) A method as in claim 13, wherein certain switches are provided to convert said I/O circuitry into either said transmitter circuitry configuration or into said receiver circuitry configuration.

Claims 25-38: Cancelled

39. (New) A device comprising a plurality of integrated circuits (ICs) and further comprising multi-mode Input/Output (I/O) circuit for transmitting and receiving data between at least two ICs, where each of the at least two ICs contains at least one of said I/O circuits, comprising at least one of transmitter circuitry or receiver circuitry, said transmitter circuitry sending data to receiver circuitry in another IC, and said receiver circuitry receiving data from transmitter circuitry in another IC, said I/O circuit being constructed with CMOS-based transistors that are selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, or as a single differential current or voltage mode link.

40. (New) A device as in claim 39, where said transmitter circuitry sends data to said receiver circuitry in another IC over a first pair of adjacently disposed conductors, and where said receiver circuitry receives data from said transmitter circuitry in another IC over a second pair of adjacently disposed conductors.

41. (New) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating under a condition where a power supply voltage of said transmitter circuitry is equal to a power supply voltage of said receiver circuitry in another IC, for operating under a condition where the power supply voltage of said transmitter circuitry is less than the power supply voltage of said receiver circuitry in another IC, and for operating under a condition where the power supply voltage of said transmitter circuitry is greater than the power supply voltage of said receiver circuitry in another IC.

42. (New) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in one of a plurality of double single-ended, CMOS voltage level link modes, wherein in a first mode a power supply voltage of said transmitter circuitry is equal to a power supply voltage of said receiver circuitry in another IC, wherein in a second mode the power supply voltage of said transmitter circuitry is less than the power supply voltage of said receiver circuitry in another IC, and wherein in a third mode the power supply voltage of said transmitter circuitry is greater than the power supply voltage of said receiver circuitry in another IC.

43. (New) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in one of said plurality of double single-ended, CMOS voltage level link modes, or in said differential voltage or current mode links, and wherein the ICs at each end of the link may operate with different supply voltages.

44. (New) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a double single-ended voltage mode link

mode.

45. (New) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a double single-ended current mode link mode.

46. (New) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a mode defined by a single differential voltage mode link with a single-ended input drive.

47. (New) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a mode defined by a single differential voltage mode link with a differential input drive.

48. (New) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a mode defined by a single differential current mode link with a single-ended input drive mode.

49. (New) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a mode defined by single differential current mode link with a differential input drive.

50. (New) A device as in claim 39, where certain switches are provided to convert said I/O circuitry into either said transmitter circuitry configuration or into said receiver circuitry configuration.

51. (New) A device as in claim 39, where at least one of said plurality of ICs comprises a radio frequency IC, and where at least one other one of said ICs comprises a baseband IC.